Reverse Engineering of Intel's Branch Prediction

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17.11.2023

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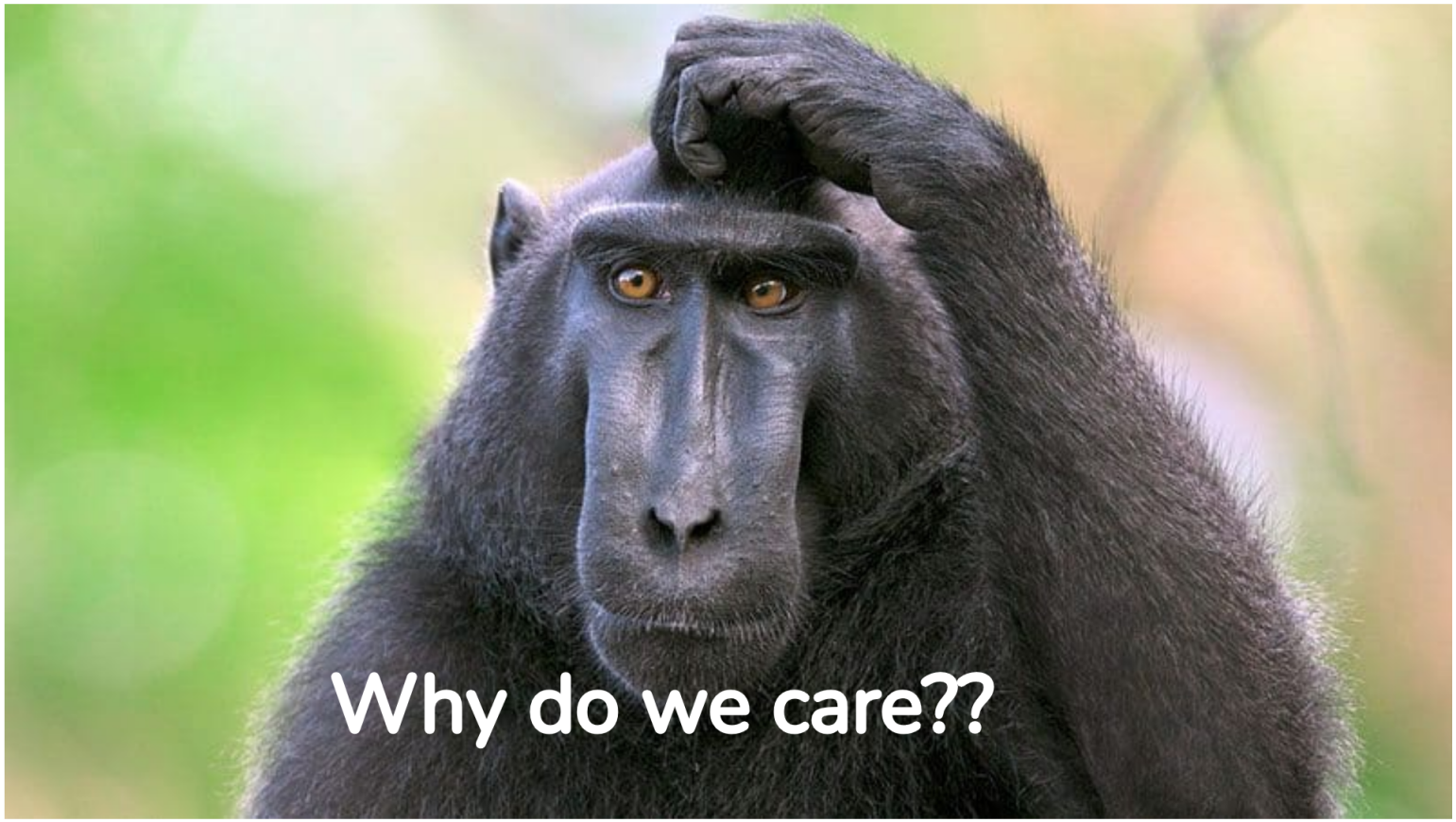


Branch Prediction

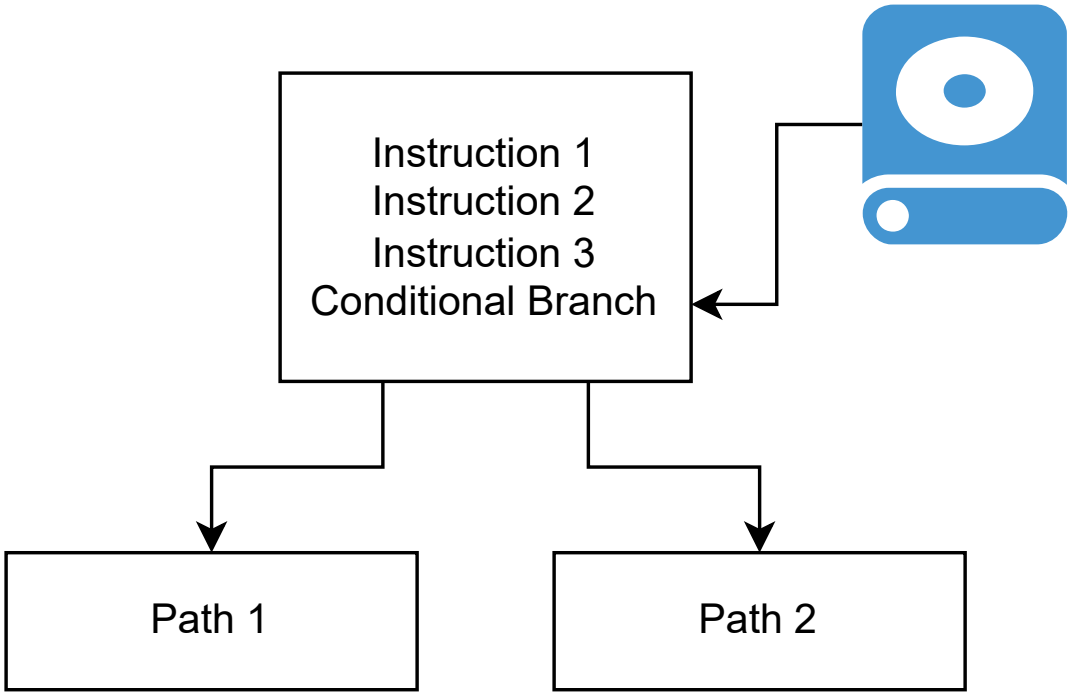
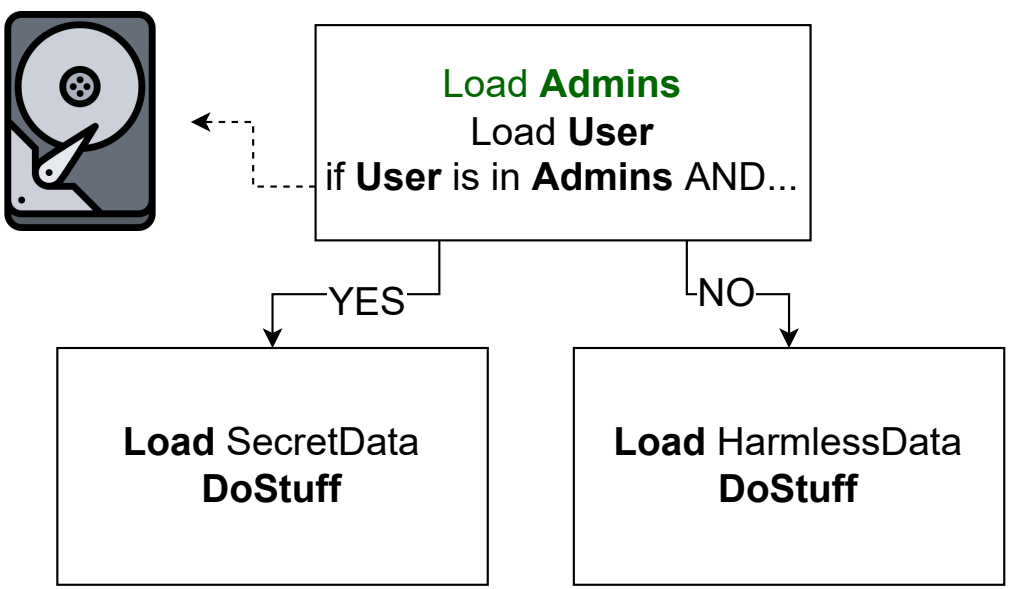


Figure: High level graph representation of a conditional branch.

Speculative Execution



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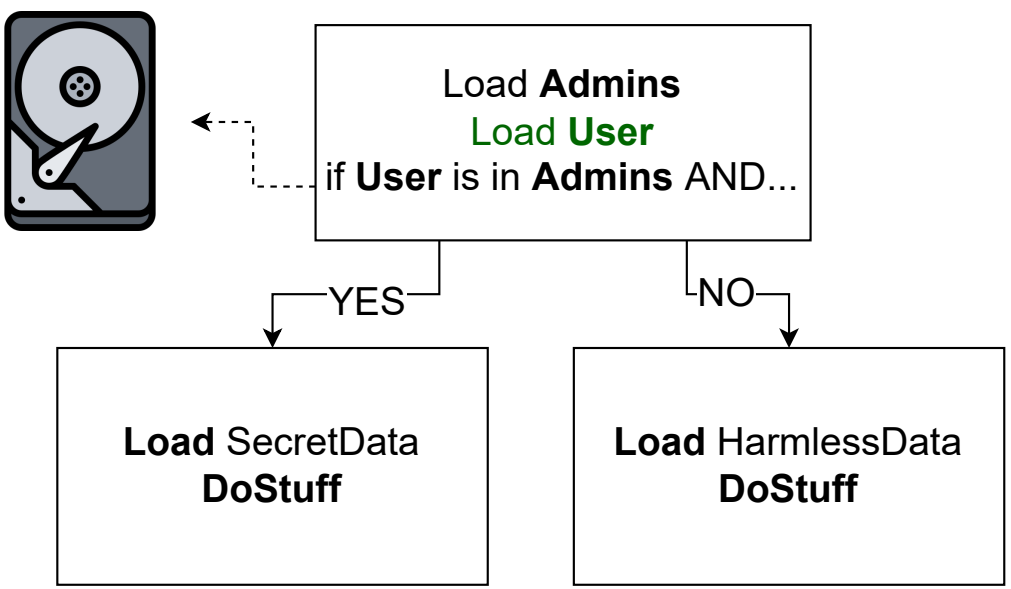
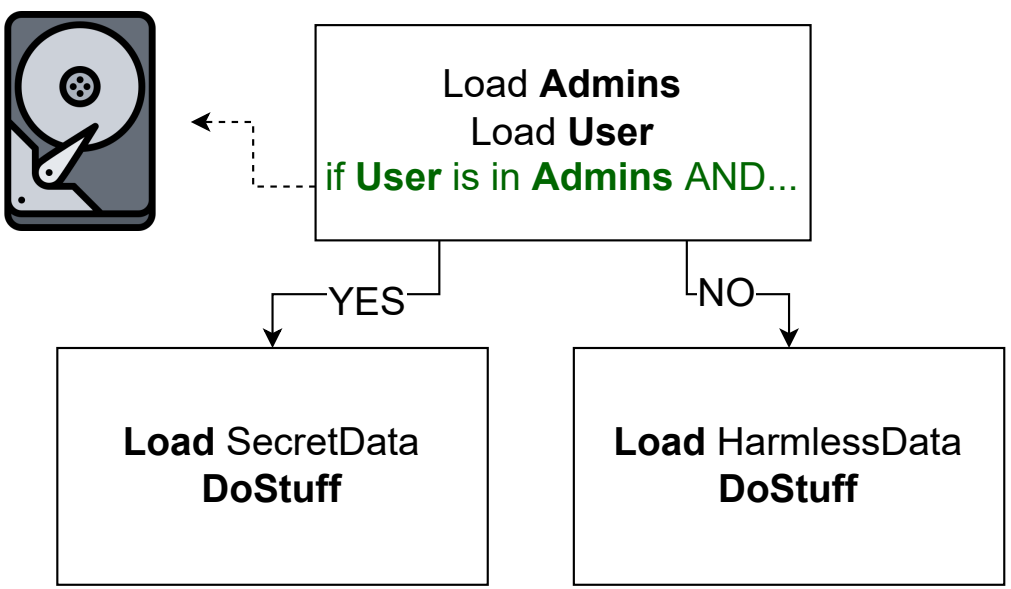


Registers/Flags
EAX: 0x17A2BC77
EBX: 0x00000000
ECX: 0x00000000

Speculative Execution



Registers/Flags
EAX: 0x17A2BC77
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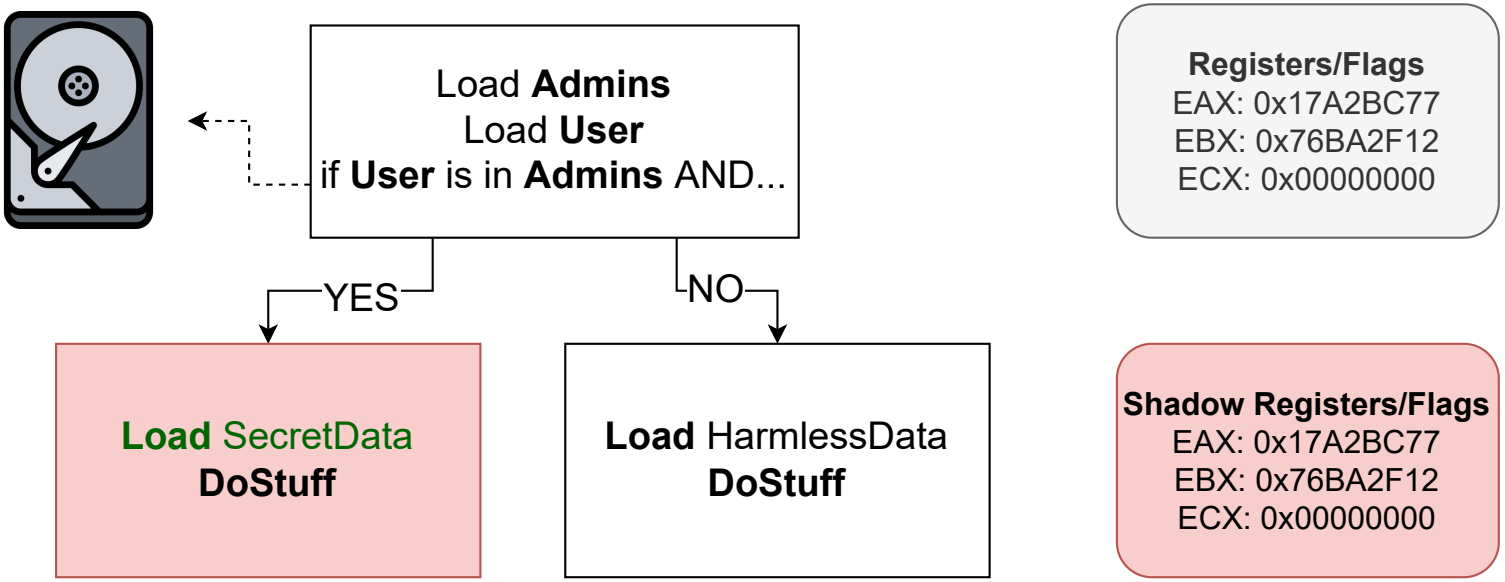

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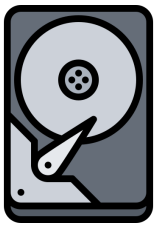


Load **Admins**
Load **User**
if **User** is in **Admins** AND...

YES

Load SecretData
DoStuff

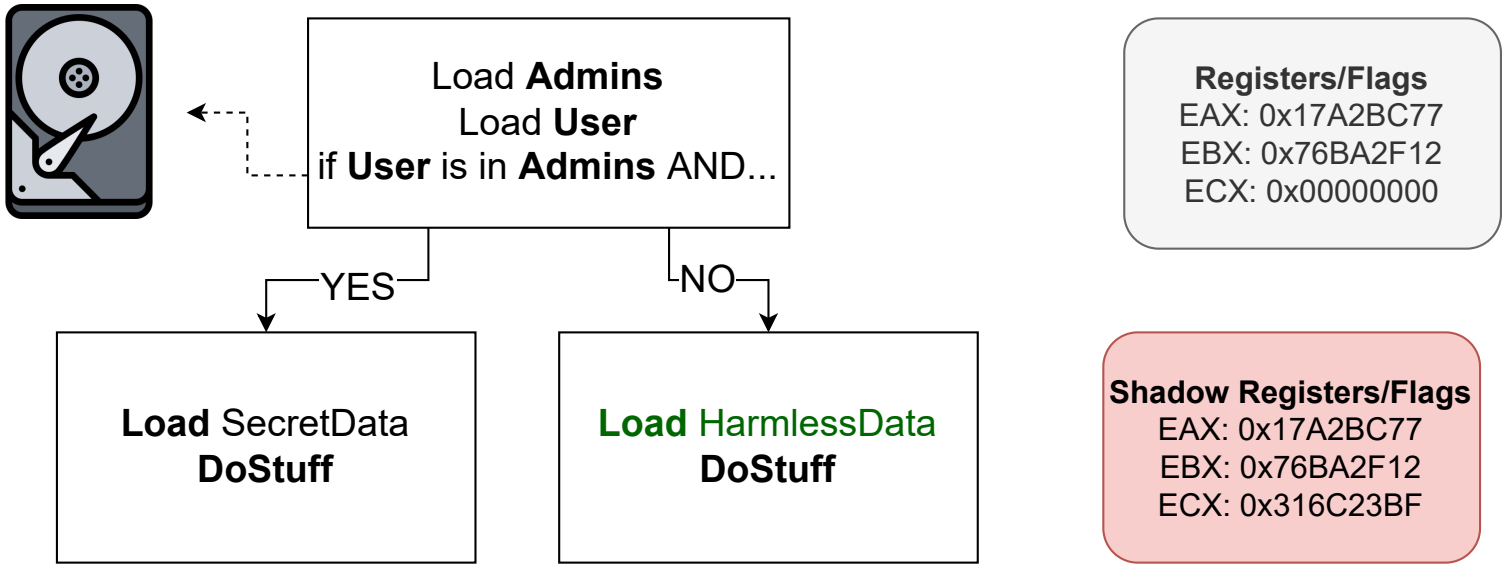
NO

Load HarmlessData
DoStuff

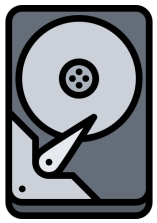
Registers/Flags
EAX: 0x17A2BC77
EBX: 0x76BA2F12
ECX: 0x00000000

Shadow Registers/Flags
EAX: 0x17A2BC77
EBX: 0x76BA2F12
ECX: 0x316C23BF

Speculative Execution



Speculative Execution



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Shadow Registers/Flags
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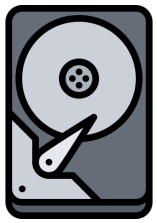
Cache
Admins
User

Speculative Execution



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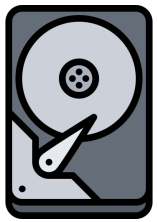

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Admins
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SecretData

Attacker Scenario

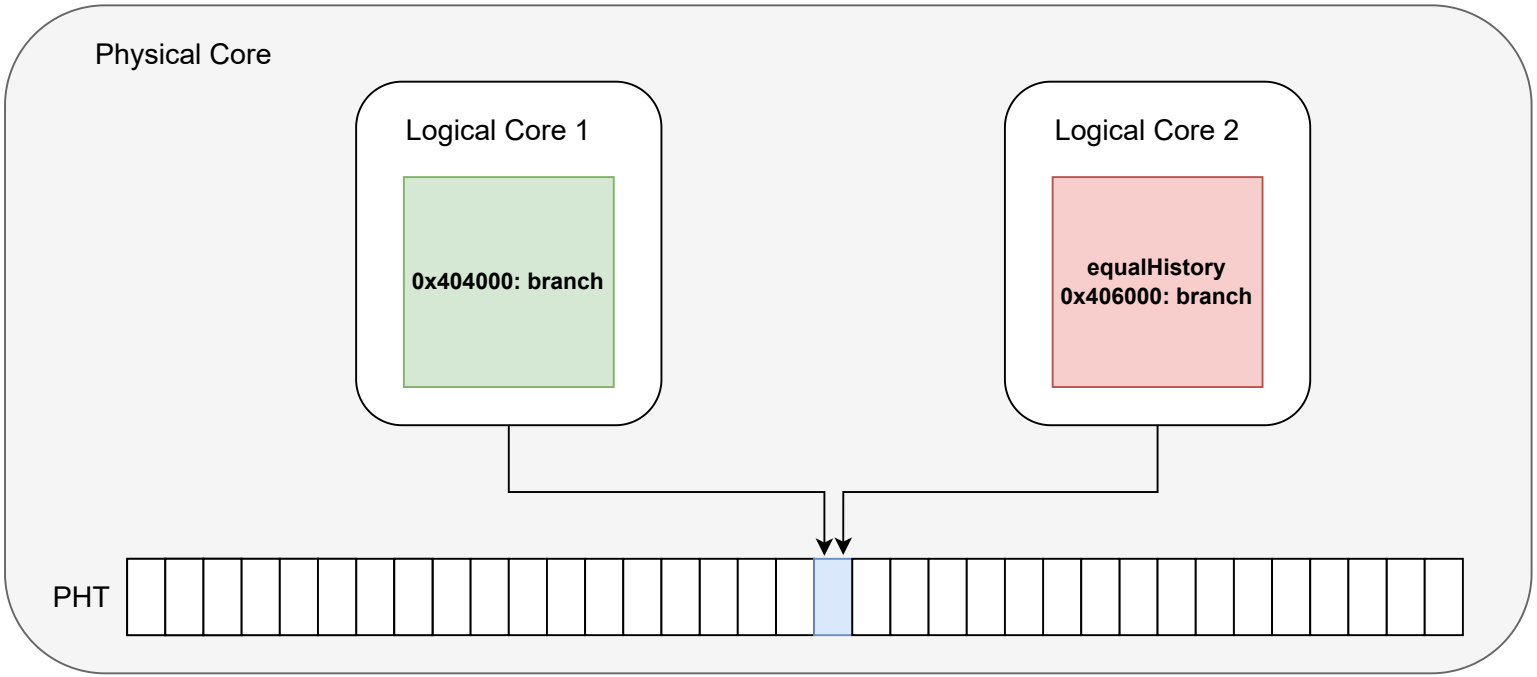


Figure: Attack scenario [CBS+19, KHF+19].

PHT Indexing

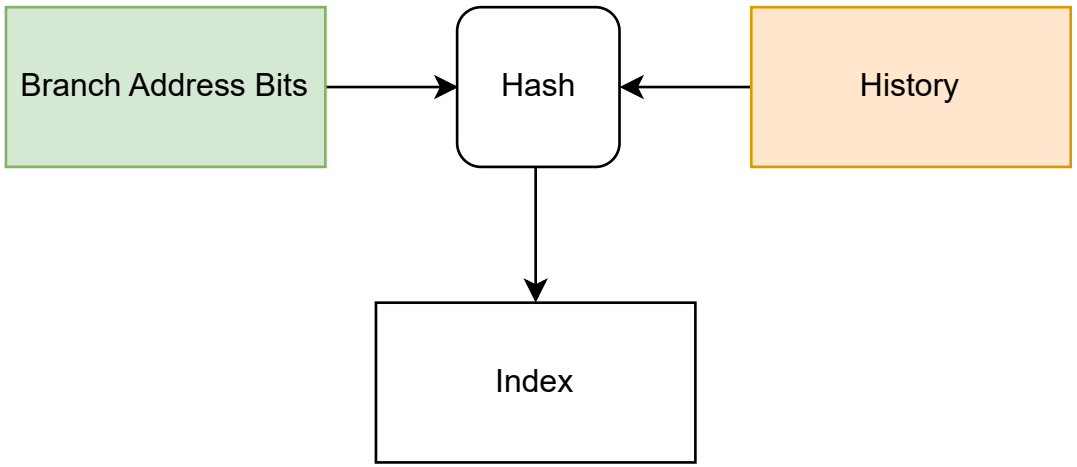


Figure: High level hash function for PHT indexing

Injector & Target Setup

Algorithm 1: *Target* program that gets mistrained by the *injector*

```
1 setCore(6)
2 while experimentOn do
3     normalizeHistory()
4     //Not taken
5     if True then
6         nop
```

Algorithm 2: *Injector* program

```
1 setCore(14)
2 while experimentOn do
3     normalizeHistory()
4     //Taken
5     if False then
6         nop
```

Result

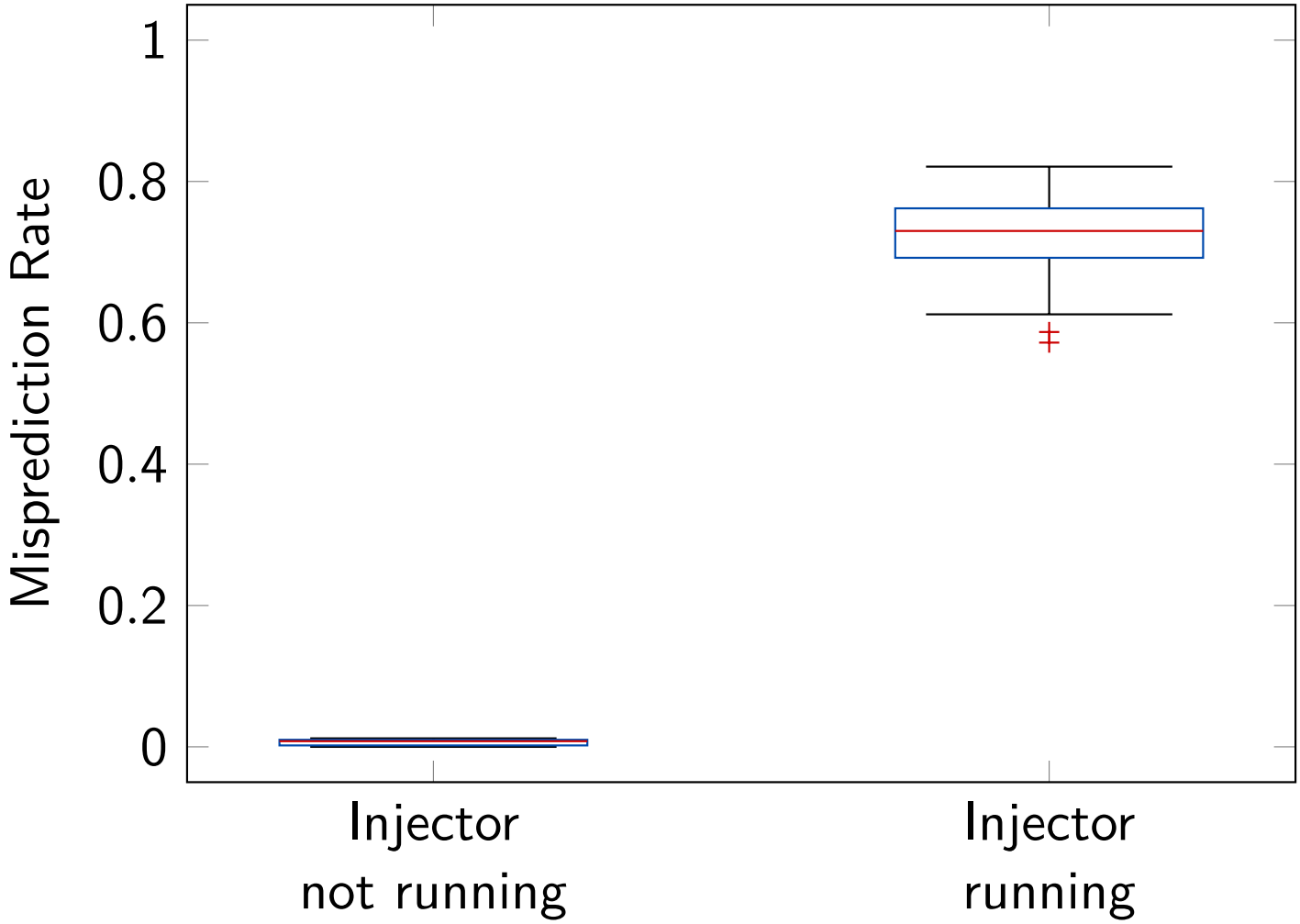


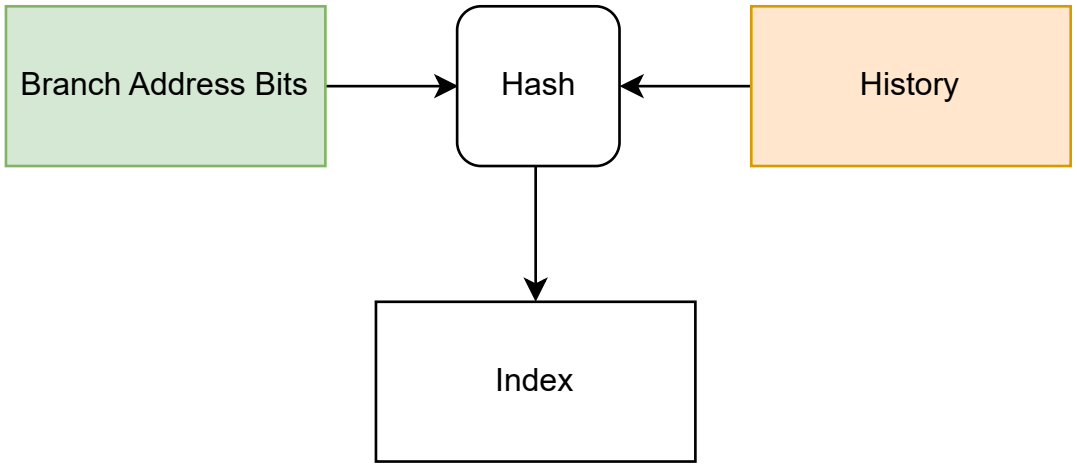
Figure: The mispredicts of the spy branch in the *target* go up when the *injector* runs. Thus, it successfully mistrains the *target's* branch.

What we know:

- Each PHT entry has a 2-bit/3-bit saturating counter
- Logical cores on the same physical core share branch prediction units
- A history impacts PHT indexing
- All branches affect the history except for not taken conditional branches
- The history stores the last 93 branches [YTN+23]

Reverse the Hash Function

- Normalize history
- Increase address of injector branch by one each iteration
- Collect all colliding branches



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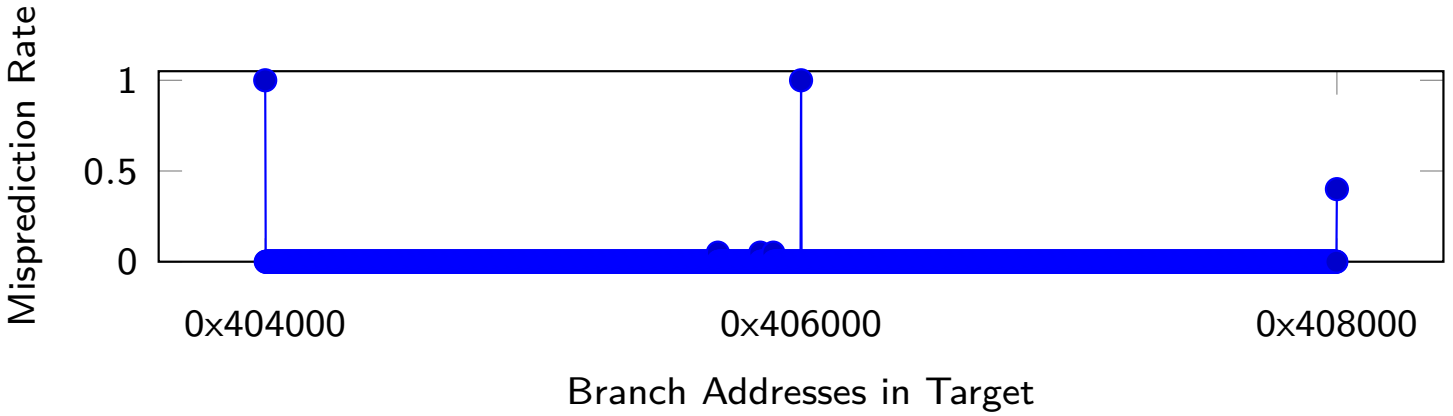
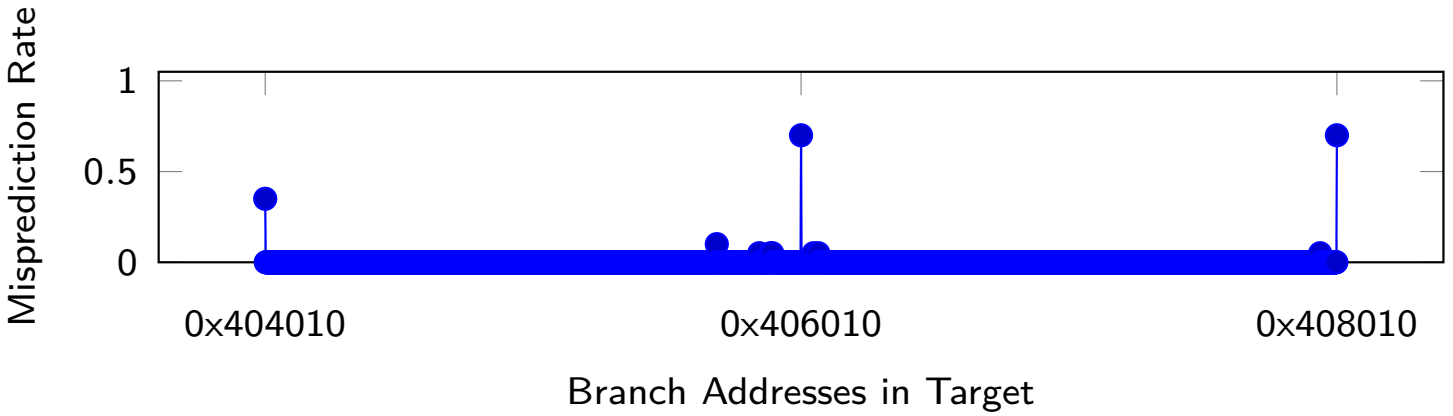
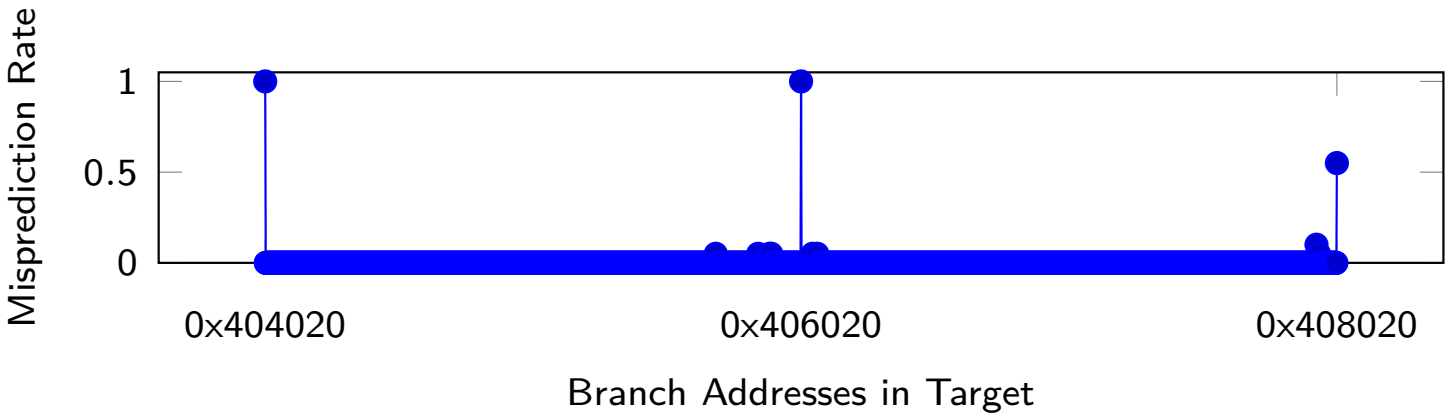
Reverse the Hash Function







Spectre PoC (Proof of Concept)

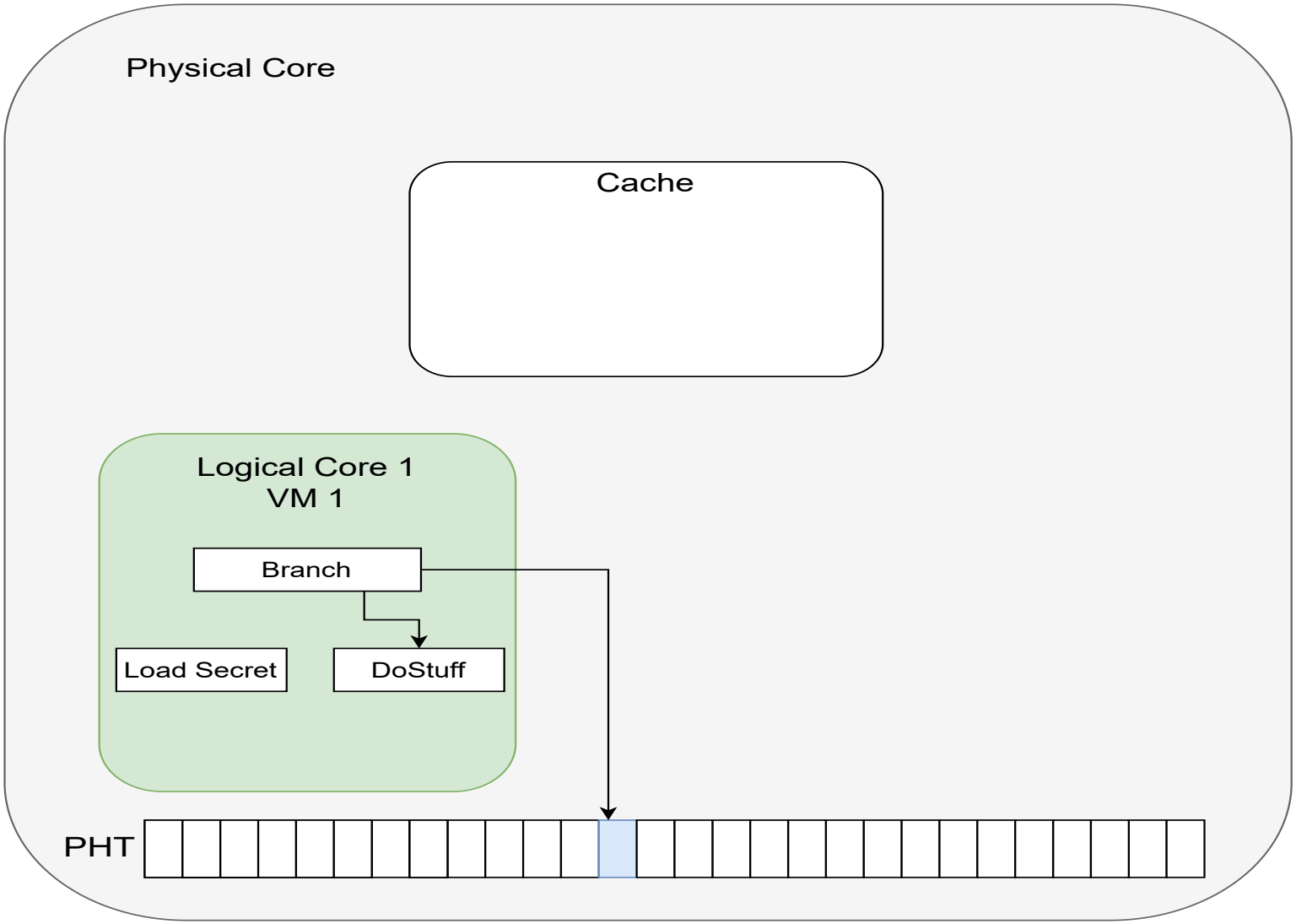


Figure: Spectre PoC (Active)

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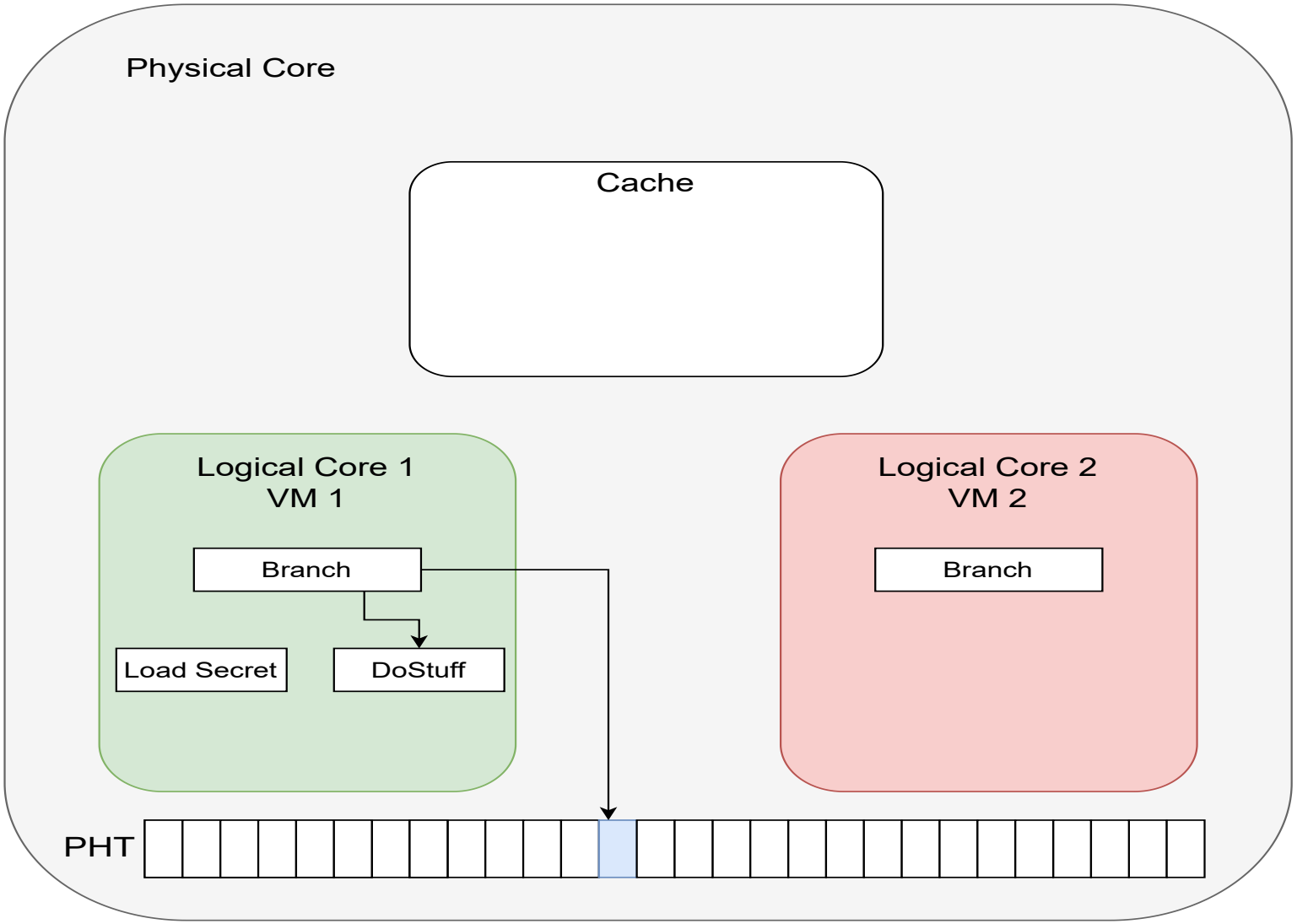

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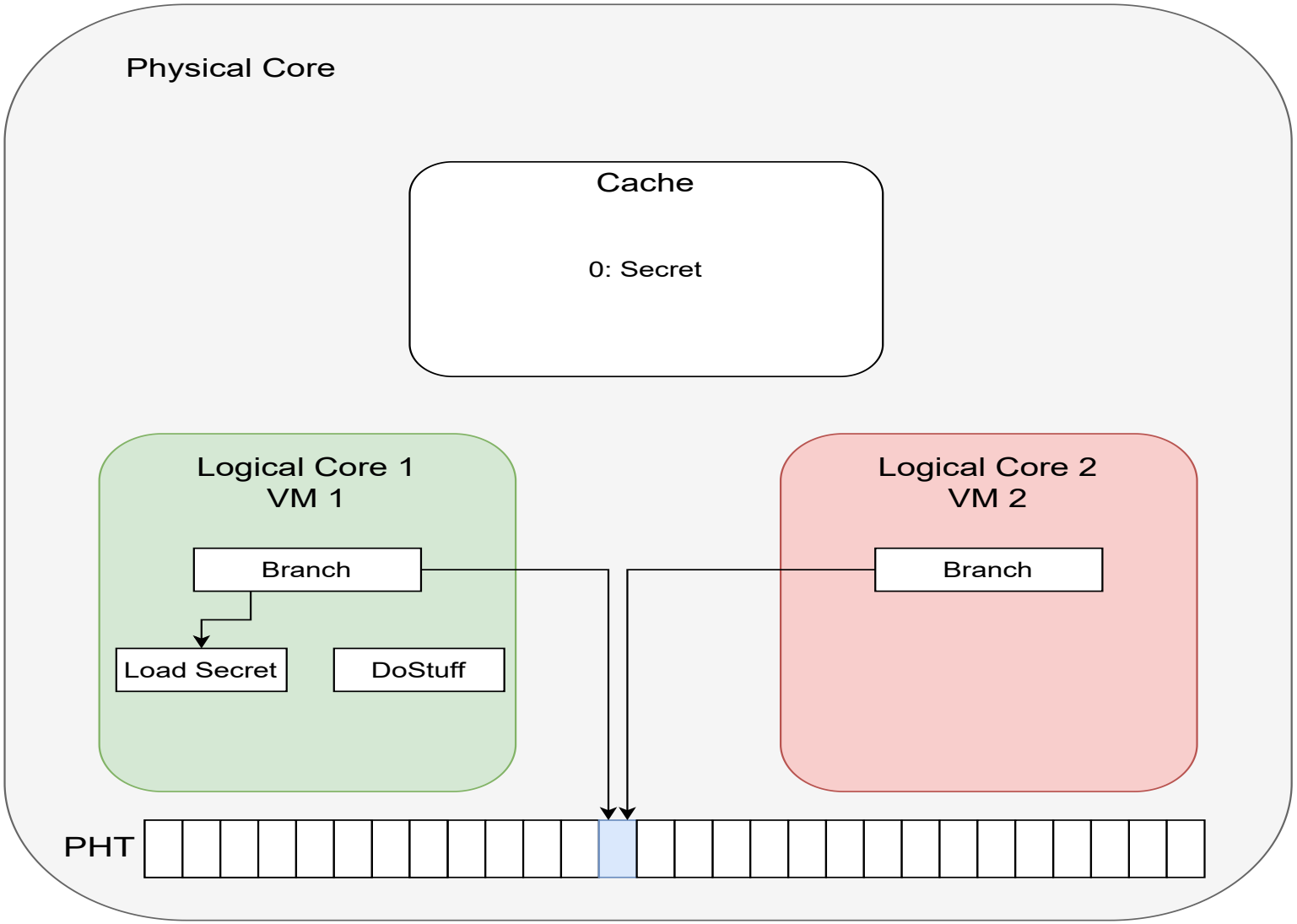

Figure: Spectre PoC (Active)

Leakage on the same logical core

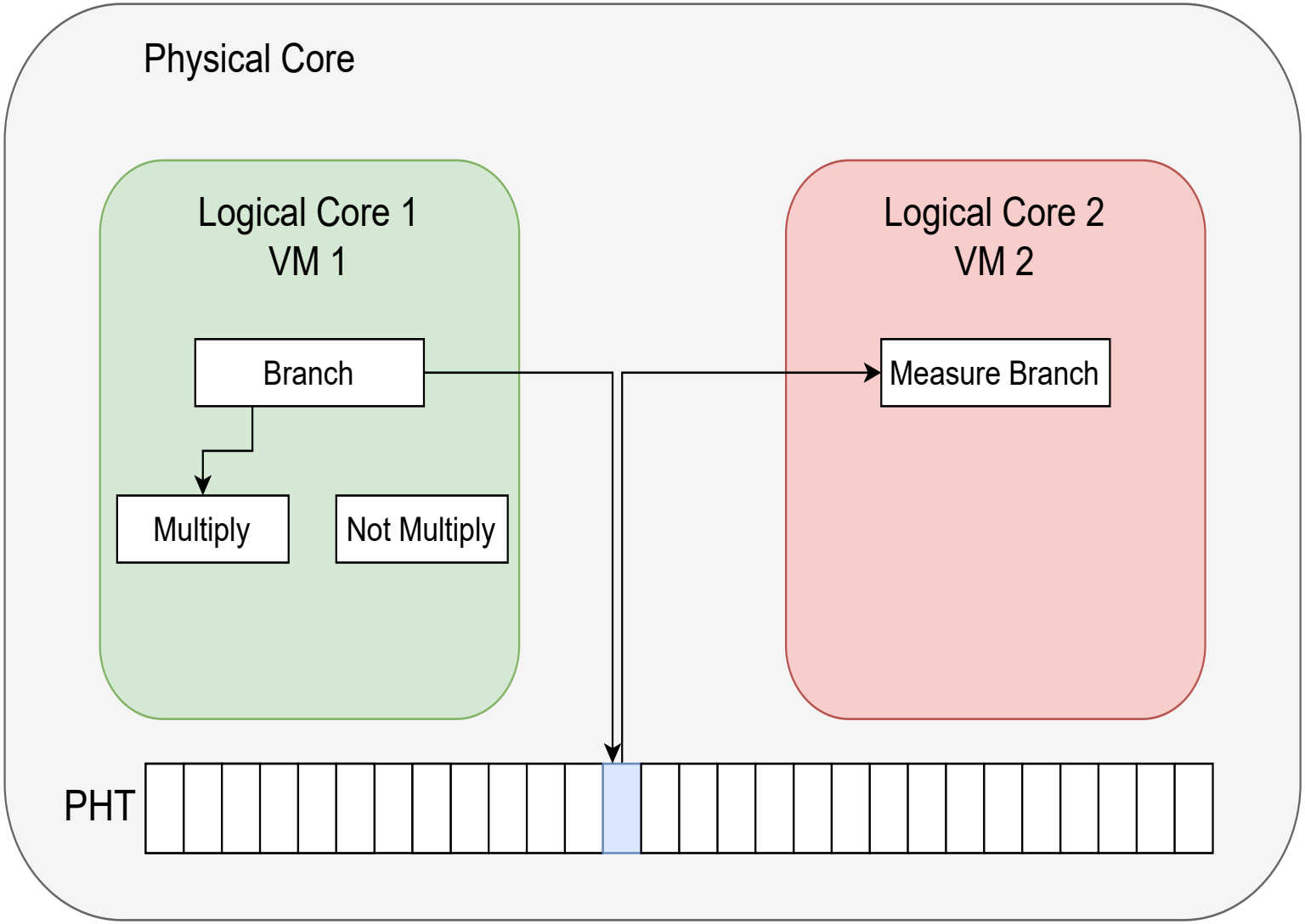

Figure: Spectre PoC (Passive)

Conclusion

- Attacks mostly theoretical yet
- Learning: Avoid shared resources
- Knowledge on branch prediction can help with defense measures

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- Learning: Avoid shared resources
- Knowledge on branch prediction can help with defense measures

References I

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Hosein Yavarzadeh, Mohammadkazem Taram, Shravan Narayan, Deian Stefan, and Dean Tullsen.
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In *44th IEEE Symposium on Security and Privacy, SP 2023, San Francisco, CA, USA, May 22-26, 2023*, pages 1220–1237. IEEE, 2023.

Non-branch Instructions

Algorithm 3: *Target* program

```
1  setCore(6)
2  i ← 0
3  while experimentOn do
4      normalizeHistory()
5      instructions_1
6      //Always not taken
7      if True then
8          nop
9      i ← i + 1
10     nop_pattern...
```

Algorithm 4: *Injector* program

```
1  setCore(14)
2  i ← 0
3  while experimentOn do
4      normalizeHistory()
5      instructions_2
6      //Always taken
7      if False then
8          nop
9      i ← i + 1
```

Content of a PHT entry

Algorithm 5: Experiment pseudocode to test what kind of saturating counter is used.

```
1  param_1 ← args[0] //Assign first passed argument
2  i ← 0
3  while experimentOn do
4      normalizeHistory() //Ensures same history each iteration
5      //Cycling around the saturating counter
6      if ⌊i/param_1⌋ mod 2 then
7          nop
8      i ← i + 1
```

Content of a PHT entry

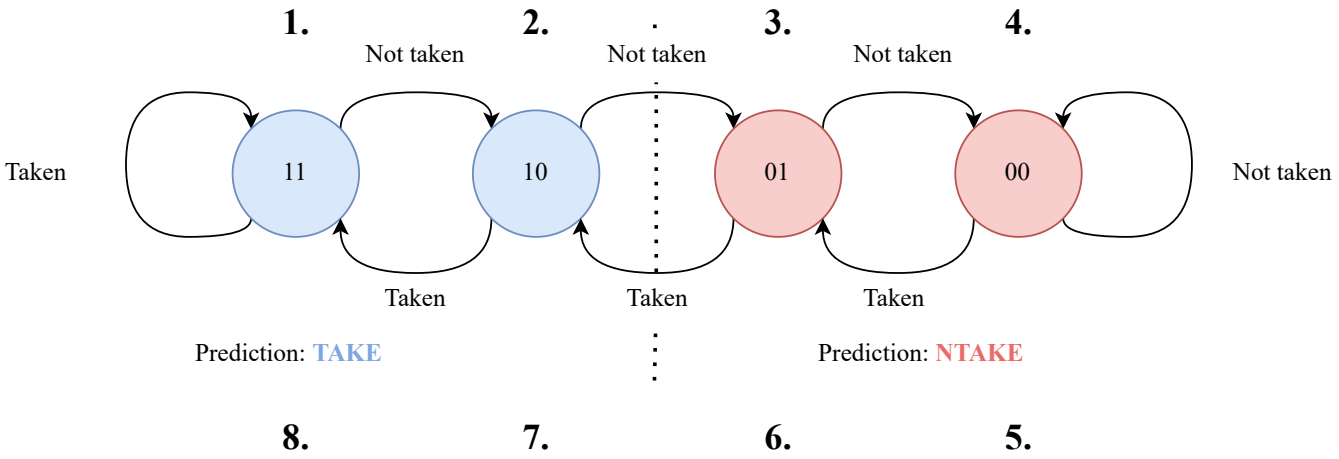

Figure: 2-bit saturating that we cycle around

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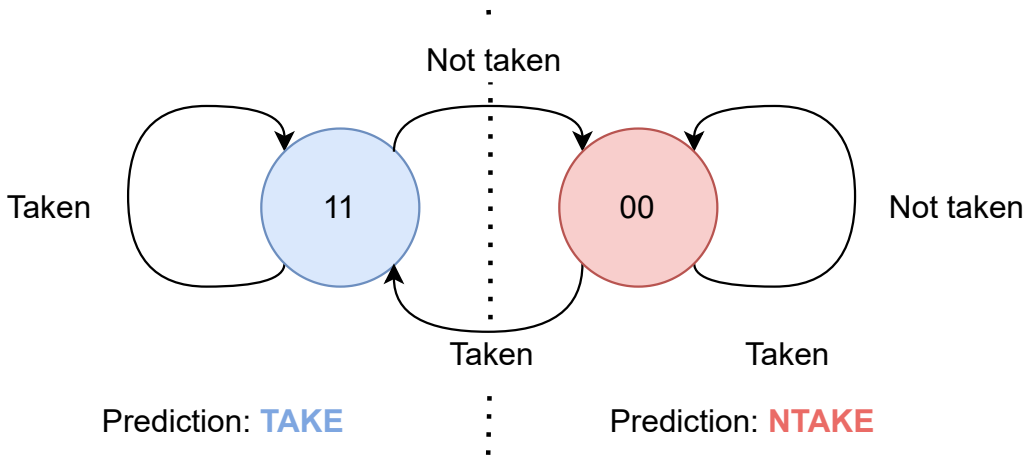

Figure: 1 Bit Counter

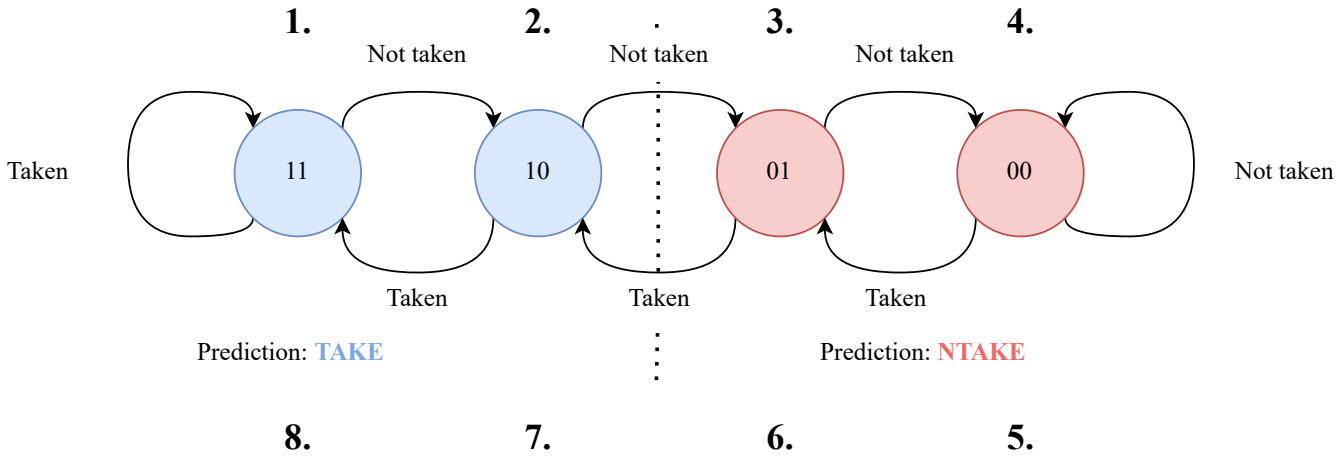

Figure: 2-bit saturating that we cycle around

Result

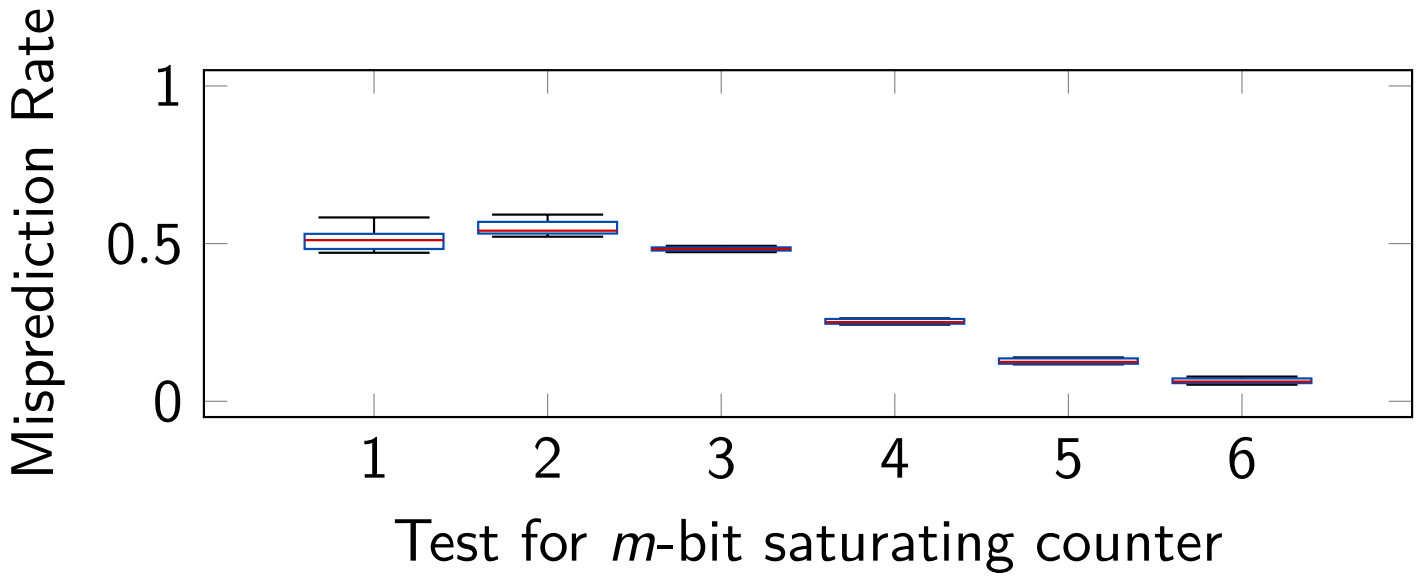

Figure: Results to show which saturating counter is used. They indicate a 3-bit saturating counter as results have a misprediction rate of around 0.5 for the first three values and then halve.

TAGE Predictor

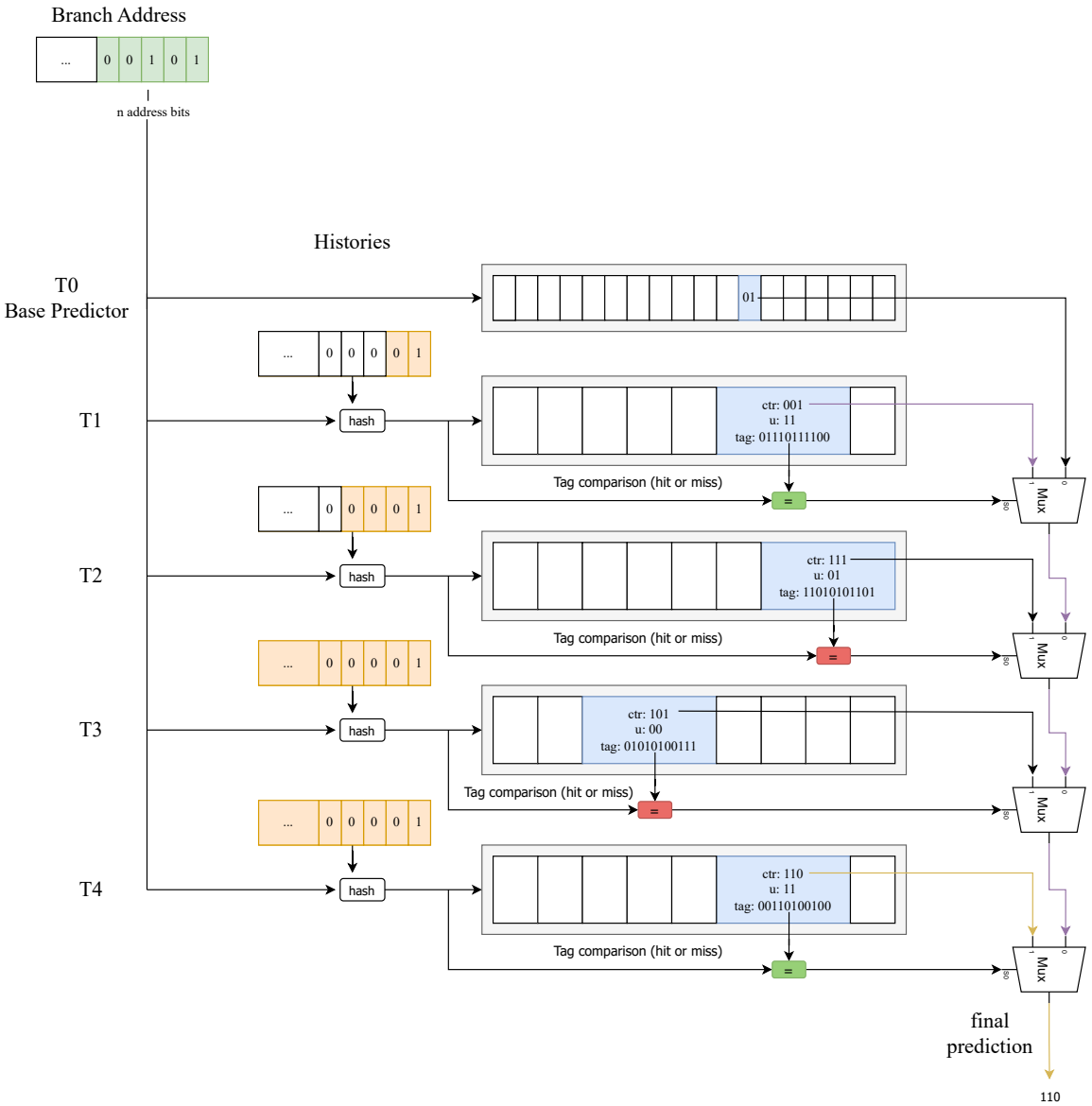

Figure: TAGE predictor illustration. Used by AMD Zen 2 processors (2019) e.g. [SM06, Sez07, Sez11]